I/O Optimizer

Reduce time-to-market and manufacturing costs of PCB systems

Today's FPGAs are very powerful devices with high pin count, numerous I/O standards and high speed capabilities. In addition, advanced implemented logic in the FPGA very often requires that hundreds of logical signals be mapped to physical signals. In effect, this is a real challenge for electrical engineers to match the HDL world with the electrical world.

In light of these challenges, Mentor Graphics' xDX IOPT (I/O Optimizer) provides an extensive set of functionalities created to fully support Schematic and PCB engineers with their FPGA-on-Board integration. xDX IOPT is proved to significantly reduce the time-to-market of PCB systems as well as reducing manufacturing costs, both key to today's fast paced and ever-changing environment.

Creating or optimizing the FPGA is made possible at any stage of the project using a dedicated FPGAs tab in the xDX Designer schematic tool. Schematic/layout and xDX IOPT databases are kept in sync through a traffic light based Synchronization assistant. This allows users to better control the project's design data flow.
In addition, schematic users can decide when the FPGA data (new as well as updated one) is to be transferred to the PCB design. Before placement or routing is even started on the PCB, xDX IOPT allows floor planning to be performed on the Xpedition project data. This is carried out using the xDX IOPT Floorplan window for better initial assignment and then results can be exported to Xpedition Layout. FPGA parts are managed at either the project or the enterprise library level.

The integration with the Xpedition Enterprise design flow is an example of one of the many benefits that xDX IOPT offers:

- Bridges the domains of HDL based FPGA design and PCB design
  - Automated, fast and error free bidirectional information exchange
- Fully integrated, easy to use FPGA on board optimization reduces layer count, cost and design cycle time
- Correct-by-construction FPGA Vendor rule driven I/O assignment
- Fast, easy and automated FPGA symbol generation saves days of PCB design creation time
- Fast and error free optimization cycle through the schematic update process

- Integrated floor planner
  - Improves component placement around the FPGA
  - Optimizes routing inside and outside the FPGA
- Optimization based on actual PCB layout data
  - Supports un-routed, partially routed traces including BGA breakout traces
- Better results by optimization across the multiple FPGA devices
- Comprehensive library of FPGA vendor devices
- On-demand service guarantees the very latest device support
  - Average new device turnaround time is less than a week
  - Free of charge to customers on maintenance
  - Covers not yet released devices