FPGA I/O Designer

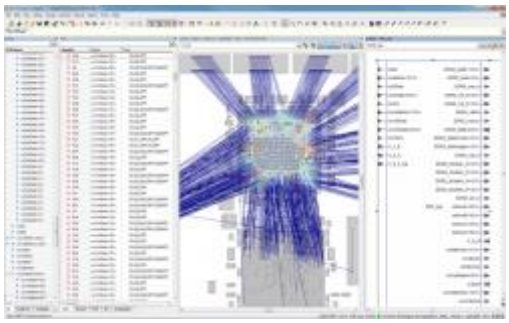
Optimize FPGA I/O for PCB placement & routing

Overview

Xpedition® xDX I/O Designer eliminates the barriers between FPGA and PCB design organizations, enabling concurrent design processes with greater accuracy and speed.

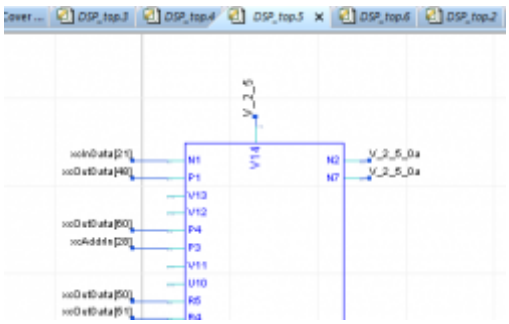
It provides correct-by-construction FPGA I/O assignment, allowing pin swapping and layout-based I/O optimization within the PCB process, delivering these benefits:

Reduces the total product design cycle time by changing a serial process into a concurrent process
Decreases PCB manufacturing costs by eliminating PCB signal layers
Eliminates PCB re-spins due to out-of-date FPGA symbols on the PCB
Enables high-speed performance optimization
Removes the costs associated with creating and maintaining the FPGA symbol(s) for the PCB schematic



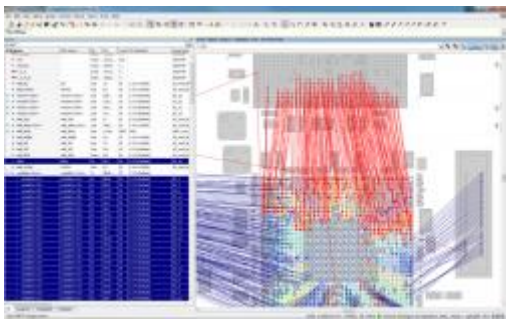
Fully optimized for concurrent design

Enables FPGA/PCB co-design processes



Fast and easy PCB symbol and schematic creation

Quickly convert an FPGA design into a PCB schematic that's ready for layout



Improve I/O accuracy

Reduce board layers, shorten traces, reduce vias

Technical Specifications

- Supports the latest FPGA vendor devices
- Bi-directional I/O optimization and pin-swapping based on actual PCB layout component orientation
- Built-in I/O assignment rules specific to each device, simplifying pin assignments
- Uses the generic FPGA symbol/symbol set from your corporate library, or allows you to create custom sets for a specific FPGA design
- Identifies and documents which signal connections are made to device pins and how they map to original board-level bus structures
- Manages data consistency between flows, automatically generating updated FPGA place and route constraints
- Easy-to-use drag-and-drop graphical interface that updates on the fly
- Imports LMS, EDIF and XML schematic symbols
- Supported FPGA vendors: Actel, Altera, Lattice, Xilinx