Constraint Management

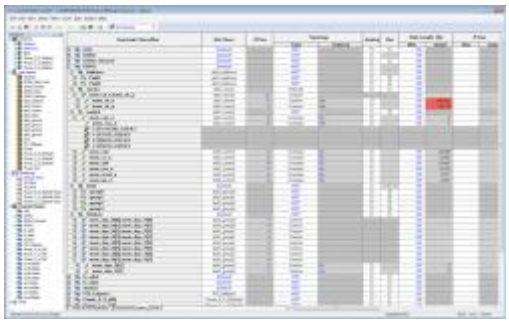
A fully integrated, constraint-driven design methodology

Overview

Constraint Manager, formerly Constraint Editor System (CES), provides a common, integrated constraint definition environment for schematic capture and layout.

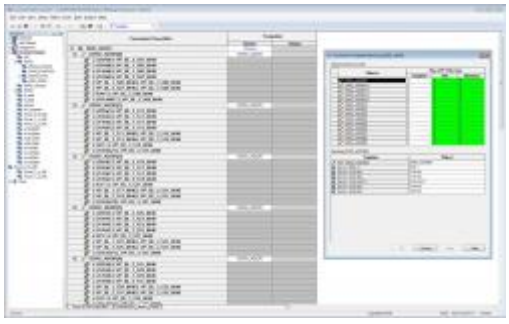
Bi-directional cross-probing, highlighting and selection between the constraint environment, design capture, and layout ensure design intent is accurately, efficiently captured and adhered.

The constraint manager supports definition and verification of electrical and physical constraints within one environment, eliminating the need for separate databases, and simplifying a complex constraint entry process while improving design accuracy. Constraint reuse within a design and between designs, and support for concurrent constraint entry accelerate the design process.



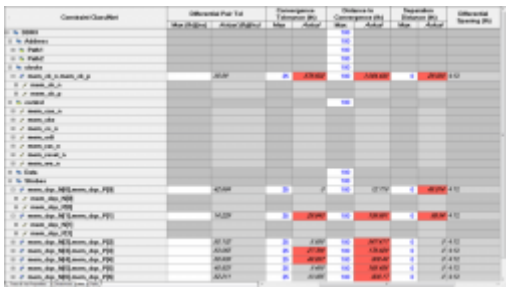
Single, integrated constraint entry tool for performance and manufacturability constraints

Provides common, concurrent constraint editing and cross-probing from design entry through PCB layout



Constraint templates enable application of complex rules to multiple nets

Ensure transfer of design intent from the simulation environment directly to layout



Constraints can be verified directly within the constraint editing environment

Validate layout against design intent

Technical Specifications

- Powerful and easy-to-use spreadsheet-like GUI guided by the design database and cross probing to applications
- Hierarchical constraint entry speeds input of complex rules on many objects
- Architecture allows multiple simultaneous edits using locking mechanisms to prevent concurrent users from editing the same data
- Speeds time-to-market with informal and formal constraint reuse, concurrent constraint entry, and editing
- Improves design productivity with embedded applications allowing in-tool constraint editing
- Users can create a topology and associated constraints with virtual pins or they can use the more sophisticated automatic topologies
- Provides easy to use functions for finding invalid model assignments, model overrides or mismatches between device and model information
- Preserves rules throughout the flow for net renames, connectivity additions/removals, pin and/or gate swaps and stack-up changes
- Users can easily create differential pairs using common naming conventions, wild card searches on net names, and information from interactive selection of pairs of nets across the entire design
- Stack-up properties can be viewed and modified to plan for proper impedance matching