

# HyperLynx Signal Integrity

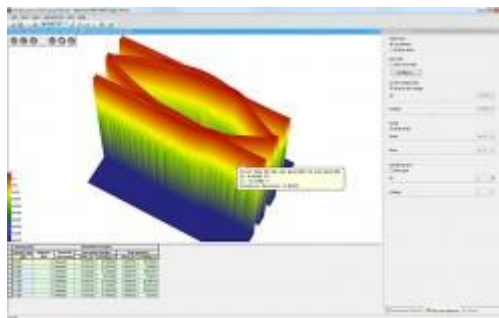
Analyze signal integrity issues early in the design cycle to eliminate costly re-spins

## Overview

HyperLynx® Signal Integrity generates fast, easy and accurate signal integrity analysis in PCB systems design.

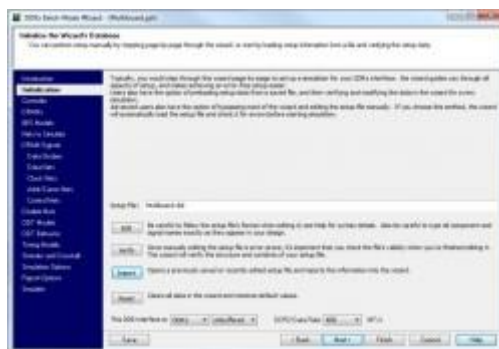
HyperLynx SI helps engineers efficiently manage rule exploration, definition and validation, ensuring that engineering intent is fully achieved.

The software is tightly integrated into the design flow, from schematic design through final layout verification.



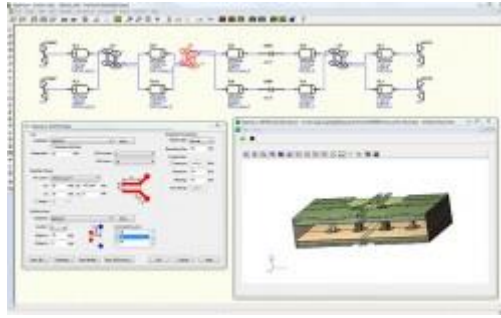
## Comprehensive SERDES support

Includes FastEye diagram analysis, S-parameter simulation, and BER prediction



## DDRx wizard

Simplifies setup and verification of DDR-protocol memory systems, including timing



### **Integrated full-wave 3D electromagnetic field solver**

HyperLynx SI makes it easy to manage detailed structure analysis (including differential vias)

### **Technical Specifications**

- Industry-renowned ease of use, enabling shorter time to results
- Accurate modeling of trace impedance, coupling, and frequency-dependent losses
- Sweep different values for discretizes, trace geometries and lengths, and driver settings
- Terminator wizard recommends optimal termination strategies
- DDRx wizard allows complete verification of DDR, DDR2, and DDR3 memory systems, including timing
- Accurately predict serial interface bit error rates (BER), worst-case bit sequences, and eye diagrams in hours instead of weeks
- Advanced, exploratory via modeling
- Integrated full-wave 3D electromagnetic field solver
- Provides an early look at likely EMC failures
- Easily instantiate HSPICE, ELDO, IBIS-AMI, AMS, S-parameter, and IBIS models
- Pre-layout mode for design exploration, schematic validation and constraint definition
- Post-layout mode for full batch design verification
- Integration with the Xpedition Enterprise flow including schematic, constraint, and layout environments
- Powerful, easy to use multi-board analysis, including support for EBD models and connector models