Questa® Advanced Simulator

Questa’s core simulation and debug engine

The Questa® Advanced Simulator combines high performance and capacity simulation with unified advanced debug and functional coverage capabilities for the most complete native support of Verilog, SystemVerilog, VHDL, SystemC, SVA, UPF and UVM.

The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA and SoC designs.

Questa spans the levels of abstraction required for complex SoC and FPGA design and verification from TLM (Transaction Level Modeling) through RTL, gates, and transistors and has superior support of multiple verification methodologies including Assertion Based Verification (ABV), the Open Verification Methodology (OVM) and the Universal Verification Methodology (UVM) to increase testbench productivity, automation and reusability.

Features

High Performance and Capacity
The Questa Advanced Simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms of SystemVerilog and VHDL, improving SystemVerilog and mixed VHDL/SystemVerilog RTL simulation performance by up to 10X. Questa also supports very fast time-to-next simulation and effective library management while maintaining high performance with unique capabilities to pre-optimize and define debug visibility on a block by block basis enabling dramatic regression throughput improvements of up to 3X when running a large suite of tests. To increase simulation performance for large designs with long simulation times, Questa also has a Multi-Core option. Questa Multi-Core takes advantage of modern compute systems by partitioning the design to run in parallel on multiple CPU’s or computers using either automatic or manually driven partitions. To achieve even greater performance, Questa supports TBX; the highest performance Transaction Level link to the Veloce platform enabling a 100x increase in performance with debug visibility and a common testbench.

Assertion Based Verification

Questa delivers a comprehensive, standards-based ABV solution, offering the choice of SystemVerilog, Property Specification Language (PSL), or both. To ease the adoption of ABV, Questa also includes the Questa Verification Library (QVL). QVL is a comprehensive SystemVerilog assertion checker and monitor library that makes it easier to adopt ABV. QVL Checkers cover a wide range of design properties and is also optimized for formal verification and emulation, while QVL Monitors support a wide range of industry standard protocols for simulation.

Test Automation

The Questa Advanced Simulator supports the most comprehensive solutions for testbench automation in the industry. In addition to the tight integration with Questa inFact for intelligent testbench automation, the Questa Advanced Simulator enables the automatic creation of complex, input-stimulus using Stimulus scenarios described in terms of constraints and randomization using SystemVerilog or SystemC Verification (SCV) library constructs.

Questa combines all of these forms of stimulus generation with functional coverage to identify the functionality exercised by the automatically generated stimulus. Using functional coverage metrics (SVA or PSL) as feedback for test creation, engineers can adjust constraints to focus random testing on coverage holes. This automation methodology offers huge productivity improvements compared to handcrafting hundreds of directed tests. Questa collects all coverage data — code coverage, assertions, formal, and functional coverage — into a single highly efficient Unified Coverage DataBase (UCDB) and makes them available in real-time within the testbench or for post-processing with Questa Verification Management.

Questa Verification Management

The application of constrained-random test stimulus and metrics-driven verification dramatically increases the amount of data generated in the verification process. Questa Verification Management analyzes coverage and verification data, providing up-to-date information on the status of verification test suites and insight into how to improve the efficiency and effectiveness of the verification process. Please refer to the Verification Manager page for more detailed information.

Integrated Multi-Language Debugging

The Questa debug environment fully supports all standard languages, and its GUI usage model is consistent across all languages and abstraction levels. Questa automatically recognizes key objects in the design and verification environment, providing intuitive ways to view and debug these objects. For example, finite state machines (FSM) are inferred, and an FSM debug window provides a natural way to visualize the current state and state transitions of the FSM over time.

Verification environments that are constructed with the OVM/UVM class libraries are automatically recognized and OVM/UVM Aware and SystemVerilog class based debugging is available throughout all debug windows in addition to a dedicated UVM window for unique UVM items such as configurations and streams. Questa helps automate the often time-consuming and tedious process of tracing connectivity and causality from an observed error to the root cause of the bug. This tracing can be through either a graphical schematic view or source based dataflow, the source and sink (driver and reader) relationships can be easily traversed to identify the origin of a bug.

Power Aware Verification

The management of power consumption is critical for many applications. The techniques required to manage power present unique design and verification challenges. Questa's Power Aware Simulation, combined with Accellera's Unified Power Format (UPF) standard, mitigates the risks of implementing low power silicon designs by accurately modeling low power silicon behavior early in the design cycle. Please refer to the Power Aware Simulation page for more detailed information.

Benefits

- High-performance, multi-language engine for the most sophisticated regression suites
- Highly productive advanced verification solution with verification management for coverage closure of large, complex electronic systems
- Easy to use, fast time-to-debugthrough native assertions and a complete multi-abstraction and multi-language debug environment including transaction-level debug
- Constrained-random stimulusgeneration to automate test development
- Native advanced SystemVerilog testbench capabilities with OVM and UVM combined with unique debug function to ease the development and debug of advanced testbenches
- High bandwidth Transaction Level (TBX) integration with the Veloce Platform to achieve dramatic simulation acceleration
- Native support of Power Aware Simulation using UPF
- Multi-Core simulation which supports all design languages and constructs and either automatically or manually partitions the design to run in parallel while maintaining a single database for debug and coverage.