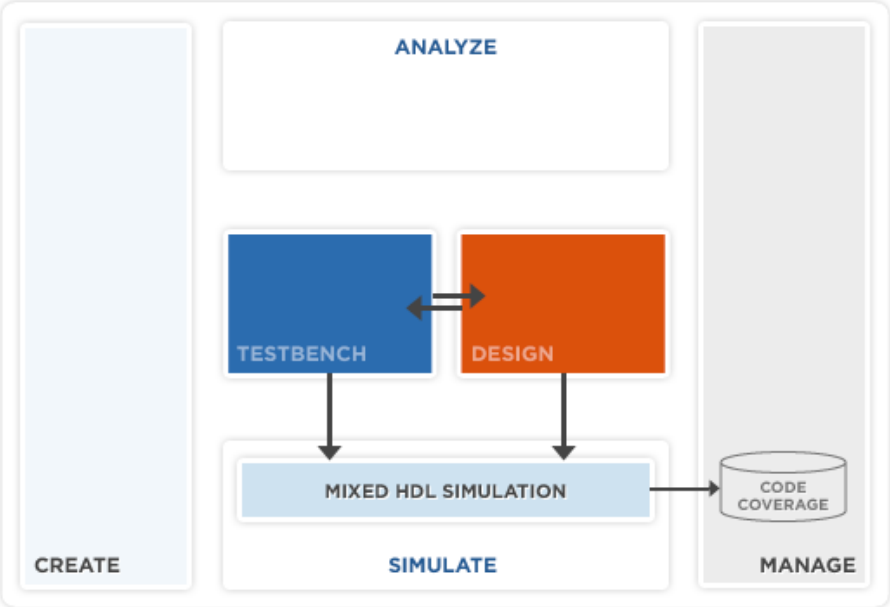
ModelSim®



Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and SystemC. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim® the simulator of choice for both ASIC and FPGA designs. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

Overview

Unified mixed language simulation engine for ease of use and performance
Native support of Verilog, SystemVerilog for design, VHDL, and SystemC for effective verification of sophisticated design environments
Fast time-to-debug, easy to use, multi-language debug environment
Advanced code coverage and analysis tools for fast time to coverage closure
Interactive and Post-Sim Debug available so same debug environment used for both
Powerful Waveform compare for easy analysis of differences and bugs
Unified Coverage Database with complete interactive and HTML reporting and processing for understanding and debugging coverage throughout your project
C**oupled with HDL Designer and HDL Author** for complete design creation, project management and visualization capabilities

Features

Advanced Code Coverage

ModelSim's advanced code coverage capabilities and ease of use lower the barriers for leveraging this valuable verification resource.

The ModelSim advanced code coverage capabilities provide valuable metrics for systematic verification. All coverage information is stored in the Unified Coverage DataBase (UCDB), which is used to collect and manage all coverage information in a highly efficient database. Coverage utilities that analyze code coverage data, such as merging and test ranking, are available. Coverage results can be viewed interactively, post-simulation, or after a merge of multiple simulation runs. Code coverage metrics can be reported by instance or by design unit, providing flexibility in managing coverage data.

The coverage types supported include:

- **Statement coverage**: number of statements executed during a run
- **Branch coverage**: expressions and case statements that affect the control flow of the HDL execution
- **Condition coverage**: breaks down the condition on a branch into elements that make the result true or false
- **Expression coverage**: the same as condition coverage, but covers concurrent signal assignments instead of branch decisions
- **Focused expression coverage**: presents expression coverage data in a manner that accounts for each independent input to the expression in determining coverage results
- **Enhanced toggle coverage**: in default mode, counts low-to-high and high-to-low transitions; in extended mode, counts transitions to and from X
- **Finite State Machine coverage**: state and state transition coverage

Mixed HDL Simulation

ModelSim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Comprehensive support of Verilog, SystemVerilog for Design, VHDL, and SystemC provide a solid foundation for single and multi-language design verification environments. ModelSim's easy to use and unified debug and simulation environment

provide today’s FPGA designers both the advanced capabilities that they are growing to need and the environment that makes their work productive.

Effective Debug Environment

The ModelSim debug environment’s broad set of intuitive capabilities for Verilog, VHDL, and SystemC make it the choice for ASIC and FPGA design.
ModelSim eases the process of finding design defects with an intelligently engineered debug environment. The ModelSim debug environment efficiently displays design data for analysis and debug of all languages.

ModelSim allows many debug and analysis capabilities to be employed post-simulation on saved results, as well as during live simulation runs. For example, the coverage viewer analyzes and annotates source code with code coverage results, including FSM state and transition, statement, expression, branch, and toggle coverage.

Signal values can be annotated in the source window and viewed in the waveform viewer, easing debug navigation with hyperlinked navigation between objects and its declaration and between visited files.

Race conditions, delta, and event activity can be analyzed in the list and wave windows. User-defined enumeration values can be easily defined for quicker understanding of simulation results. For improved debug productivity, ModelSim also has graphical and textual dataflow capabilities.

ADVANCED VERIFICATION

For advanced verification capabilities such as SystemVerilog class-based testbench, functional coverage, and UVM support, find out more about our highest performance simulation solution: Questa®